# InP/InGaAs DHBTs with 341-GHz $f_T$ at high current density of over 800 kA/cm$^2$

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## Abstract

We describe MOVPE-grown InP/InGaAs DHBTs with a 150-nm-thick collector. The collector current blocking at the base/collector heterointerface is perfectly suppressed by the compositionally step-graded structure even at collector current density of over 1000 kA/cm$^2$. A cut-off frequency $f_T$ of 341 GHz is obtained at high collector current density of 833 kA/cm$^2$ with practical on-state breakdown characteristics. This is the highest $f_T$ ever reported for any bipolar transistors.

## Introduction

For 100-Gbit/s-class ICs using heterojunction bipolar transistors (HBTs), high current density operation is essential [1]. Recently, ultrahigh-speed InP-based HBTs with cut-off frequency $f_T$ of over 300 GHz have been demonstrated [1,2], and a record $f_T$ of 305 GHz has been achieved at high current density $J_C$ of 320 kA/cm$^2$ [2]. High $J_C$ is achieved by decreasing collector layer thickness, because the maximum $J_C$ is limited by the Kirk effect. Thinning the collector is also effective for reducing the carrier transit delay $\tau_F$, and thereby increasing $f_T$. However, a thin collector causes problems, such as low breakdown voltage [1] and increased collector charging time due to large collector capacitance $C_{BC}$.

This paper describes an InP/InGaAs HBTs with a 150-nm-thick collector. To keep a practical breakdown voltage for such a thin collector, we employed double heterojunction transistor (DHBT) structure with wide band-gap InP collector. In DHBTs, it is essential to suppress the current blocking effect (which is caused by the conduction-band discontinuity at the base/collector interface) in order to achieve high $J_C$ operation. We applied a step-graded collector design [3] to suppress the current blocking. We also minimized the collector charging time by reducing both $C_{BC}$ and the series emitter and collector resistances. To reduce the $C_{BC}$, a base-pad-isolation structure [4] was utilized, which can eliminate the capacitance at the base-pad area.

## Device structure and fabrication

Fig. 1 shows the equilibrium energy-band diagram of the fabricated DHBTs. The layers were grown on a Fe-doped semi-insulating 3-inch (100) InP substrate by low-pressure MOVPE. The InP emitter layer was relatively highly doped to $6 \times 10^{17}$ cm$^{-3}$ to compensate for the space charge of electrons under high-$J_C$ operation. The base layer was 30-nm-thick InGaAs heavily doped to $6 \times 10^{19}$ cm$^{-3}$. Carbon was used as the p-type base dopant to ensure device reliability. The collector was compositionally step-graded with a thin InGaAsP layer to suppress the collector current blocking at the InGaAs /InP heterointerface, as shown in Fig.1. The band-gap energy of the inserted InGaAsP layer was 1.0 eV and the total collector thickness was 150 nm. To obtain the practical on-state breakdown voltage, the subcollector layer was also made of InP, which has much better thermal conductivity compared to InGaAs. The thickness of the emitter and subcollector layers was designed so as to minimize the series resistance.

Fig. 2 is a photograph of a fabricated DHBT with a $0.8 \times 3$ μm$^2$ emitter before passivation. The emitter shape is hexagonal and emitter orientation is parallel to the orientation flat of the wafer to attain good reliability [5,6]. The fabrication process is simple and identical to that of our baseline HBTs [7] except for the InGaAsP layer etching. After emitter mesa etching, a high-temperature anneal was carried out to reverse the hydrogen passivation of carbon acceptors [5]. The base

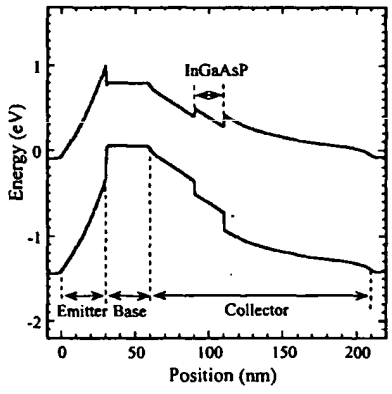


Fig. 1. Equilibrium energy-band diagram of fabricated DHBTs. A thin InGaAsP layer was inserted at the InGaAs/InP interface to suppress the collector current blocking effect.

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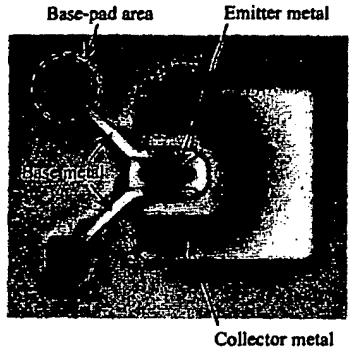


Fig. 2. I-line microscope photograph of the fabricated DHBT with a 0.8 × 3 $\mu m^2$ emitter. (Before passivation by BCB.)

sheet resistance after the anneal was 650 Ω/sq.. For the collector mesa formation, ECR-RIE was utilized to etch off the InGaAsP layer. During the wet etching for device isolation, the subcollector layers under the feed lines from the base-pad were removed by the anisotropic side-etching effect. As a result, $C_{BC}$ originating in the base-pad area is totally eliminated. After that, a fluid benzocyclobutene (BCB) was spin-coated, and the large gaps under the feed line metals were filled with the BCB after curing.

## DC performance

*Figs. 3 and 4* show Gummel plots and common-emitter I-V curves of the fabricated device, respectively. There is no degradation in turn-on characteristics even at high $J_C$ of over 1000 kA/cm$^2$. This means that the only one step of the InGaAsP layer is enough to suppress the current blocking in thin-collector DHBTs. For comparison, the I-V curves of a DHBT with 300-nm-thick collector, which was designed for 40-Gbit/s class ICs, are also plotted in Fig. 4. The thick-collector DHBT [8] has a step-graded collector structure similar to that of the 150-nm-collector DHBT. In the thick-collector DHBT, the current blocking effect occurred at $J_C$ around 100 kA/cm$^2$. In contrast, the maximum $J_C$ of the thin-collector DHBT is about ten times larger than that for the thick-collector DHBT even though the collector thickness is reduce by only half. This means that the step-graded structure is very effective for a thinner collector. The breakdown voltage of the thin-collector DHBT is lower than that of the thicker one by a factor of 1/2. However, the on-state breakdown voltage at $J_C$ = 850 kA/cm$^2$ is over 2 V for the thin-collector DHBT, which is adequate for constructing digital circuits, such as an ECL and CML.

Preliminary bias stress testing under the high-$J_C$ condition was also carried out. The test device was biased at $J_C$ = 700 kA/cm$^2$ and $V_{CE}$ = 1.5 V on wafer at room temperature. Fig. 5 shows the variation in the current gain over 4 h. In spite of the high-$J_C$ condition, the current gain stayed almost constant. This shows the possibility of stable operation of the DHBTs under an ultrahigh-$J_C$ condition.

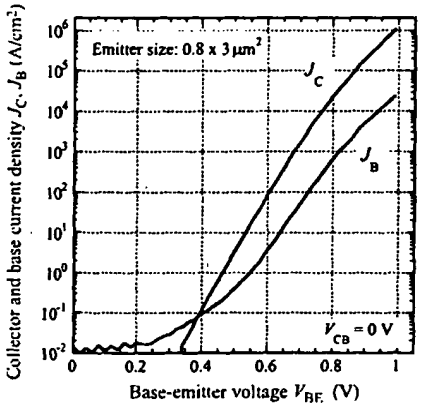


Fig. 3. Gummel plot for the fabricated DHBT with a 0.8 × 3 $\mu m^2$ emitter.

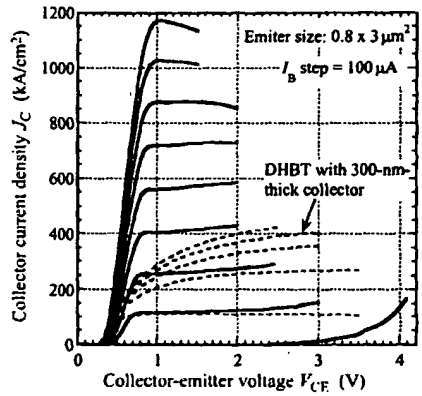


Fig. 4. Common-emitter I-V characteristics. For comparison, the I-V curves of a DHBT with a 300-nm-thick collector, which was designed for 40-Gbit/s-class ICs, are shown in the same scale.

## Microwave performance

The microwave performance of the fabricated DHBTs was characterized by on-wafer *S*-parameter measurements from 0.5 to 50 GHz using a HP8510C network analyzer. Fig. 6 shows cutoff frequency $f_T$ as a function of $J_C$ at collector-emitter voltage $V_{CE}$ of 1.2 V. The peak $f_T$ of 341 GHz is achieved at $J_C$ as high as 833 kA/cm$^2$, while the $f_T$ of the 300-nm-collector DHBT falls when $J_C$ exceeds 100 kA/cm$^2$. This is the highest $f_T$ ever reported for any bipolar transistors. The frequency dependence of current gain, Mason's unilateral gain,

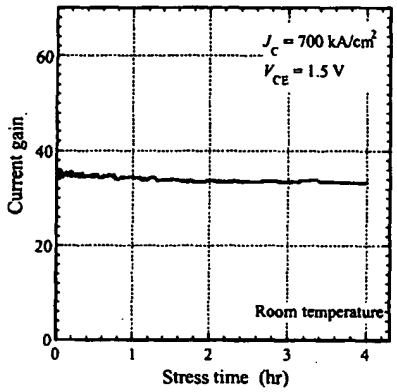


Fig. 5. Short-term stability of current gain at $J_C$ of 700 kA/cm².

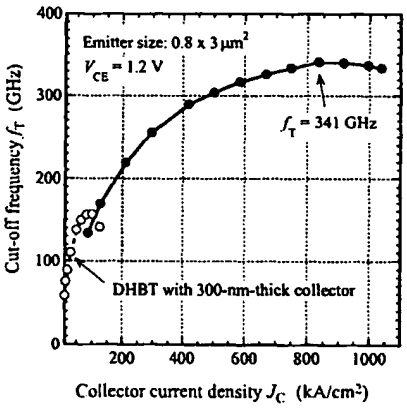


Fig. 6. Measured $f_T$ plotted as a function of collector current density. For comparision, $f_T$ of a DHBT with a 300-nm-thick collector is also shown.

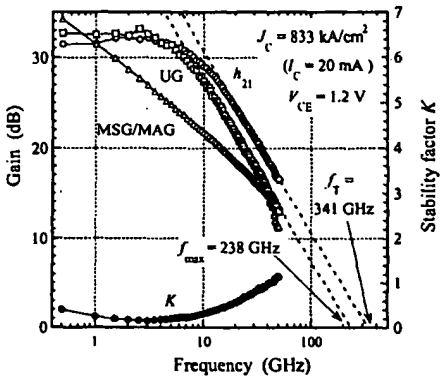


Fig. 7. Current gain, Mason's unilateral gain, maximum stable gain/maximum stable available gain, and stability factor K for the fabricatied DHBT.

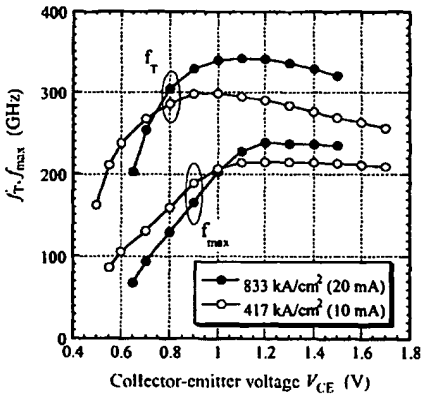


Fig. 8. Variation of $f_T$ and $f_{max}$ with collector-emitter voltage $V_{CE}$.

maximum stable gain/maximum available gain, and stability factor $K$ is shown in Fig. 7. The $f_T$ and $f_{max}$ were obtained assuming a –20-dB/decade frequency-dependence of the current gain and Mason's unilateral gain, respectively. Noteworthy is that the $f_T$ is only slightly reduced to 337 GHz at 1000 kA/cm² and $f_T$ of over 300 GHz is obtained in a wide range of $J_C$ from 500 to over 1000 kA/cm². The high-$J_C$ capability of around 1 MA/cm² is the highest for InP-based HBTs and is almost the same as that of high-speed SiGe HBTs [9]. Fig. 8 shows the dependence of $f_T$ and $f_{max}$ on $V_{CE}$, and excellent collector turn-on characteristics were obtained. The $f_{max}$ rapidly increases at $V_{CE}$ < 1 V and peaks at 1.2 V even at the current injection of 833 kA/cm². The abruptness of the carbon profile may also contribute to the quick turn-on behavior.

### Small-signal equivalent circuit analysis

From the measured $S$-parameters and the device geometry, small-signal transistor parameters were extracted, as shown in Fig. 9. The emitter resistances ($R_{EE}$ and $r_E$) and emitter junction capacitance $C_E$ were directly estimated from the dependence of the measured $S$-parameters on $J_C$. The collector resistance $R_C$ was calculated from the sheet resistance, contact resistivity, and the geometry. The other elements were extracted by numerical optimization. Good agreement was obtained between the measured and modeled $S$-parameters, as shown in Fig. 10.

In spite of the thin collector structure, the collector charging time was evaluated to be as low as 0.13 ps. This is due to the low emitter and collector resistances (5.3 and 2.3 Ω) and the reduced $C_{BC}$ enabled by the base-pad isolation structure. High-$J_C$ operation reduces the dynamic emitter resistance $r_E$ to 2.3 Ω. The carrier transit delay $\tau_F$ is only 0.26 ps, which corresponds to an average carrier velocity through the base and collector of about 4 × 10⁷ cm/s. This suggests that the thin base

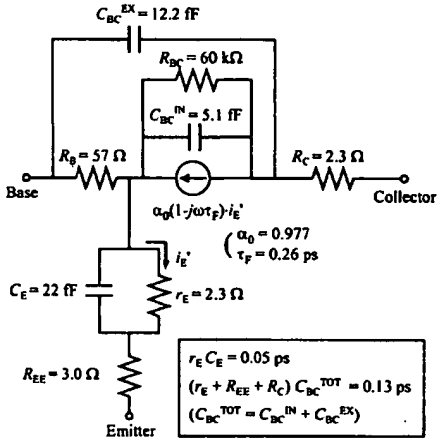


Fig. 9. Device equivalent curcuit model at $V_{CE}$ = 1.2 V and $J_C$ = 833 kA/cm².

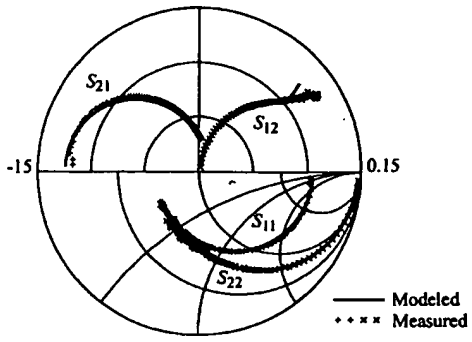


Fig. 10. Comparison of the measured and modeled $S$-parameters for $V_{CE}$ = 1.2 V and $J_C$ = 833 kA/cm², in the frequency range from 0.5 to 50 GHz. The lower part of the figure is a Smith chart with $S_{11}$ and $S_{22}$. The upper left part is a polar plot for $S_{21}$ with a radius of 15, and the upper right part is a polar plot for $S_{12}$ with a radius of 0.15.

and step-graded collector design makes full use of the superior electron-transport property of the materials. From the evaluated element values, $f_T$ of over 400 GHz is expected using the same layer structure and bias condition if we can cut the total $C_{BC}$ in half by further improving the side-etching technique.

For increasing the $f_{max}$, reducing the relatively high base resistance $R_B$ (57 Ω) and/or the intrinsic $C_{BC}$ is necessary. An emitter-width reduction by an advanced fabrication process is the most effective for that. Applying a compositionally graded base structure [10] can also reduce the $R_B$.

## Summary

InP-based DHBTs with a 150-nm-thick collector were fabricated and investigated. The collector current blocking is perfectly suppressed by the step-graded InGaAs/InGaAsP/InP collector structure even at $J_C$ of over 1000 kA/cm² with practical breakdown characteristics. A record $f_T$ of 341 GHz was obtained at high $J_C$ of 833 kA/cm². This $J_C$ capability is the best among InP-based HBTs and is comparable to that of high-speed SiGe HBTs. The equivalent circuit analysis suggests that the high $f_T$ is due to both the extremely small carrier-transit-delay and the short collector charging time. In this paper, we investigated a vertical layer structure feasible for the high $f_T$ and high $J_C$. As the next step, we will look into lateral optimization to further improve the microwave performance.

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